What is claimed is:

1. A method for manufacturing a semiconductor device, comprising the steps of:

forming a hole having a predetermined depth in a semiconductor layer of a first conductivity type, the semiconductor layer being formed on a semiconductor substrate as constituting a part of a drain region;

forming a diffusion source layer in the hole, the diffusion source layer containing impurities of a second conductivity type different from the first conductivity type;

forming a source region of the first conductivity type in a region shallower than the depth of the hole in the semiconductor layer;

forming a channel region of the second conductivity type in a region deeper than the depth of the source region in the semiconductor layer so as to be disposed between the drain region and the source region; and

heating the semiconductor substrate to a first temperature after completing the diffusion source layer forming step to diffuse the impurities of the second conductivity type from the diffusion source layer into the channel region, thereby forming a low

resistance region having a conductivity higher than that of the channel region.

2. A method for manufacturing a semiconductor device according to claim 1, wherein the diffusion source layer forming step includes a step of forming the diffusion source layer at a bottom of the hole.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the diffusion source layer forming step includes a step of forming a polysilicon film doped with impurities of the second conductivity type in the hole.

4. A method for manufacturing a semiconductor device according to claim 3, further comprising a step of forming a source deriving electrode connected to the source region,

the step of forming the source deriving electrode including the steps of:

forming an aluminum thin film on the surface of the semiconductor substrate with the polysilicon film existing in the hole after the step of heating the semiconductor substrate to the first temperature; and

heating the semiconductor substrate provided with the aluminum thin film thereon to a second temperature allowing silicon to diffuse into

aluminum.

5. A method for manufacturing a semiconductor device according to claim 1, further comprising a step of forming a scattering control layer on the diffusion source layer so as to control impurities of the second conductivity type contained in the diffusion source layer from scattering into the surrounding atmosphere in the first heating step, after the diffusion source layer forming step and before the step of heating the semiconductor substrate to the first temperature.

6. A semiconductor device comprising:

a plurality of cells each including a drain region of a first conductivity type, a channel region of a second conductivity type different from the first conductivity type and a source region of the first conductivity type stacked in this order on a semiconductor substrate so as to be capable of forming a channel in a direction of a thickness of the semiconductor substrate; and

a low resistance region of the second conductivity type having a conductivity higher than that of the channel region, the low resistance region forming a part of an inner wall of a hole formed between adjacent ones of the plurality of cells, the

low resistance region extending in an isotropic manner with respect to a predetermined region in the hole so as to be in contact with the channel region,

wherein the drain region is shared by the plurality of the cells.

7. A semiconductor device comprising:

a plurality of cells each including a drain region of a first conductivity type, a channel region of a second conductivity type different from the first conductivity type and a source region of the first conductivity type stacked in this order on a semiconductor substrate so as to be capable of forming a channel in a direction of a thickness of the semiconductor substrate; and

a low resistance region of the second conductivity type having a conductivity higher than that of the channel region, the low resistance region forming a part of an inner wall of a hole formed between adjacent ones of the plurality of cells and being in contact with the channel region,

wherein the drain region is shared by the plurality of the cells, and

wherein the size of the cell being smaller than 2μm.

8. A semiconductor device according to claim 6,

wherein the low resistance region and the source region are in contact with each other.

9. A semiconductor device according to claim 6, wherein the low resistance region and the drain region are in contact with each other.

10. A semiconductor device according to claim 6, further comprising a sourse deriving electrode being in contact with the source region and shared by the plurality of cells, wherein the low resistance region and the source deriving electrode are in contact with each other.

11. A semiconductor device according to claim 7, further comprising a sourse deriving electrode being in contact with the source region and shared by the plurality of cells, wherein the low resistance region and the source region are in contact with each other.

12. A semiconductor device according to claim 7, further comprising a sourse deriving electrode being in contact with the source region and shared by the plurality of cells, wherein the low resistance region and the drain region are in contact with each other.

13. A semiconductor device according to claim 7 further comprising a course deriving electrode being in contact with the source region and shared by the plurality of cells, wherein the low resistance region

and the source deriving electrode are in contact with each other.